EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	340	model same optical same proximity same correction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/25 11:23
S2	66	S1 and (point same function)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 20:14
S3	9	S2 and diameter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/25 16:27
S4	5	(web$based) same EDA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/25 16:29
S5	175	(web internet) same EDA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/25 16:29
S6	50	S5 and simulation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/25 16:30
S7	1364	(IP same (intellectual and property))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 09:20
S8	108	S7 and ((simulation or functional) near4 model)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 09:20

EAST Search History

S9	134	S7 and ((simulation or functional) near4 model)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 09:20
S10	23	S9 and encrypt$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/29 09:20
S11	1642	703/14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 20:14
S12	68	S11 and internet and CAD	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 20:14

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intellectual property + ((simulation model) OR | Search | Advanced Scholar Search | Scholar Preferences | Scholar Help

Scholar Results **1 - 10** of about **1,390** for **intellectual property + ((simulation model) OR (functional model**

Hardware/Software IP Protection - group of 9 » **All articles** Recent articles
M Dalpasso, A Bogliolo, L Benini - Proceedings of the 37th conference on Design automation, 2000 - doi.ieeecomputersociety.org
... Furthermore, **model encryption** only protects hardware description language ... assumption of virtual **simulation** is that ... not carry any **intellectual property**, so that ...
Cited by 10 - Related Articles - Web Search - BL Direct

Introducing core-based system design - group of 11 »
RK Gupta, Y Zorian - Design & Test of Computers, IEEE, 1997 - ieeexplore.ieee.org
... at the price of significant **intellectual property** protection risks and ... is available through circuit **simulation** inputs, such ... The basic delay **model** used in core ...
Cited by 128 - Related Articles - Web Search - BL Direct

Data security for Web-based CAD - group of 10 »
S Hauck, S Knol - Proc. of the Design Automation Conference, 1998 - doi.ieeecomputersociety.org
... Note that the Applet **model** does not include these ... Although **intellectual property** agreements may help, relying on these ... see no changes in the **simulation** behavior ...
Cited by 20 - Related Articles - Web Search - BL Direct

Blocking in a system on a chip - group of 3 »
M Hunt, JA Rowson - Spectrum, IEEE, 1996 - ieeexplore.ieee.org
... design and verify all the **functional** blocks grate ... An industry group has begun ness **model** is needed ... barriers to reusable blocks arid **intellectual property** must be ...
Cited by 33 - Related Articles - Web Search - BL Direct

Distributed file sharing: barbarians at the gates? - group of 4 »
M Macedonia, T **Simulation**, I Command, US Army, FL ... - Computer, 2000 - ieeexplore.ieee.org
... the rights and distribution of its performers' **intellectual property**. ... CHAOS Until DFS grows a business **model**, it ... of the US Army **Simulation**, Training, and ...
Cited by 11 - Related Articles - Web Search - BL Direct

Concurrent-**simulation**-based remote IP evaluation over the **internet** for system-on-a-chip design - group of 7 »
HP Wen, CY Lin, YL Lin - Proceedings of the 14th international symposium on Systems ..., 2001 - portal.acm.org
... to create a **functional model** (or **encrypted** ... Keywords Concurrent **Simulation**, **Intellectual Property** (IP), IP Evaluation ... IP (**intellectual property**) reuse has been ...
Cited by 2 - Related Articles - Web Search

IP Delivery for FPGAs Using Applets and JHDL - group of 16 »
MJ Wirthlin, B McMurtrey - Proceedings of the 40 thIEEE/ACM Design Automation .... 2002 - doi.ieeecomputersociety.org
... the default applet security **model** and requires ... latency than possible with off-site **simulation models**. ... security of the **intellectual property** contained within ...
Cited by 4 - Related Articles - Web Search - BL Direct

IP Development and Management of IP DB Enabling Efficient System-On-Chip Design - group of 2 »
Y Lee, KW Kwon, JT Kim, CD Lee - ieeexplore.ieee.org